NANOTECHNOLOGY & PHOTONICS SOCIETY ONBOARDING RECAP

Dylan Benzi - PID

Skill 0

Semiconductor Fabrication Course

PURDUE UNIVERSITY

TEXAS
The University of Texas at Austin

intel

CERTIFICATE OF COMPLETION

THIS CERTIFICATE IS AWARDED TO

Dylan Benzi

IN RECOGNITION OF COMPLETING

SEMICONDUCTOR FABRICATION 101

This certificate is evidence that you have successfully completed the Purdue University, University of Texas at Austin, and Intel Corporation sponsored Semiconductor Fabrication 101 course.

Thursday, October 29, 2026

Date

Muhammad Mustafa Hussain
Professor, ECE, Purdue University

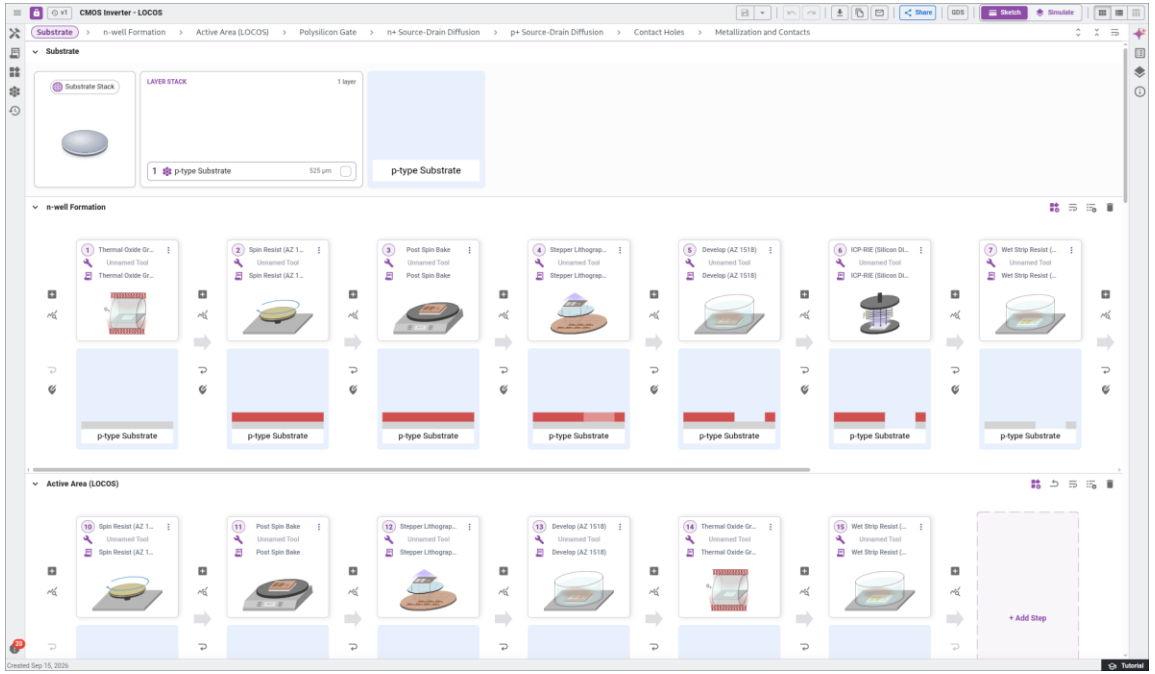
Xiuling Li
Professor, ECE, University of Texas at Austin

Skill 1

Process Flow Diagram – Fabublox

Fabublox Process

- Develop a fabrication process for a CMOS device
- Full process flow similar to industry practice
- No limitations on process used
- Split into several sections
  - n-well formation
  - Active area
  - Poly gate
  - n+/p+ Source-drain diffusion
  - Contact holes
  - Metallization + contacts

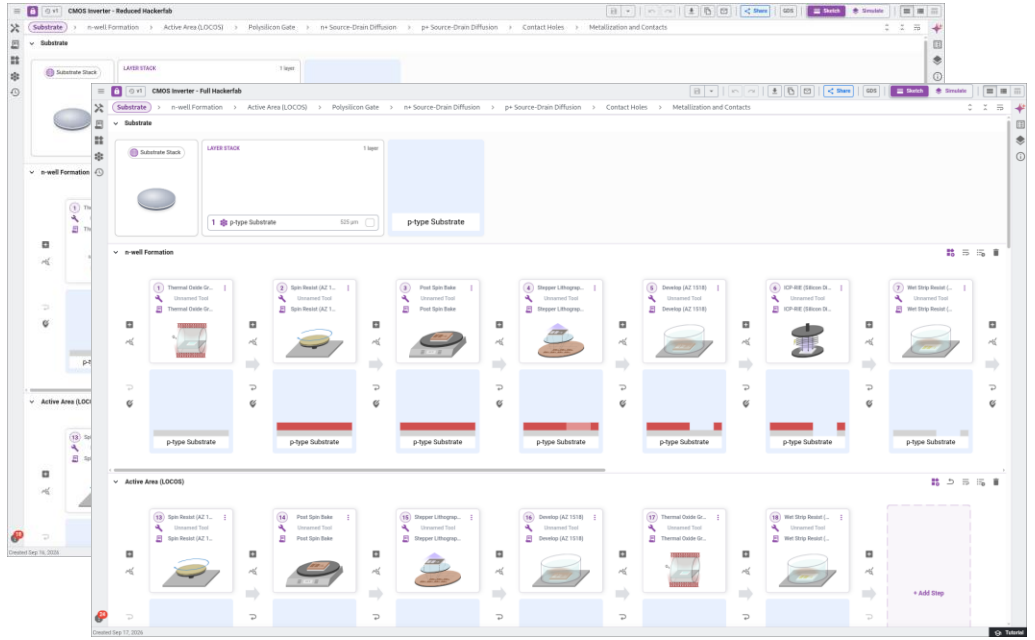




Industry-like process and output

Fabublox Hackerfab Processes

- Create two more processes
- Align with reduced and full hackerfab processes
- Restrictions on tools and processes used
- Similar restrictions to what we can manufacture here





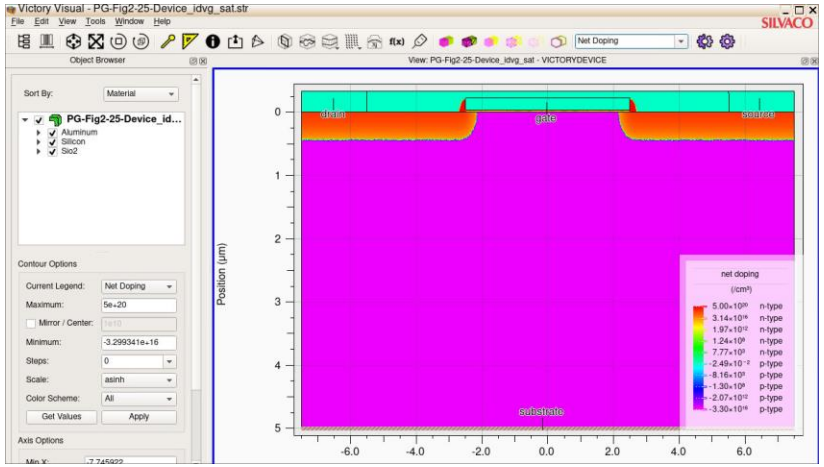
Reduced and full Hackerfab processes

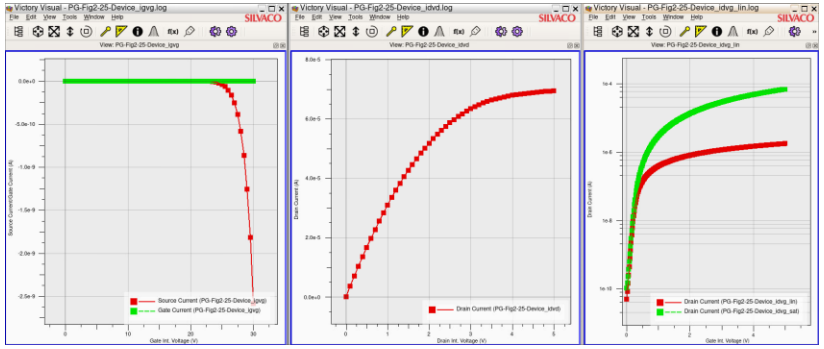
Skill 2

TCAD Device Modeling – Silvaco TCAD

Silvaco TCAD MOS Model

- Simulate the actual process implemented in skill 1
- Use Silvaco TCAD to model the process and device characteristics
- Device simulated in 2D (for now)
- Simulates etching, doping, deposition, etc.
- Once process is complete, test device characteristics
  - Gate leakage current
  - Output characteristics
  - Transfer characteristics





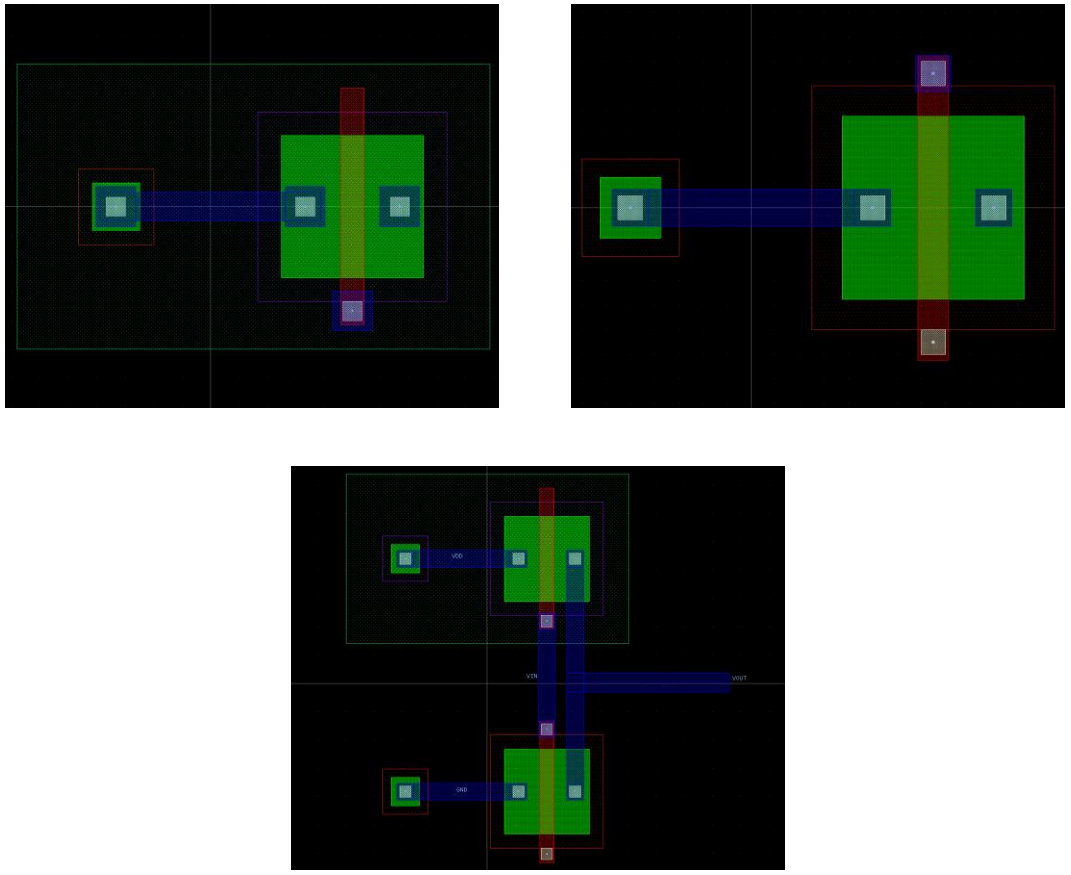
Net doping and electrical tests

Skill 3

Mask Layout and SPICE Simulation – Klayout and xschem

Device Layout with Klayout

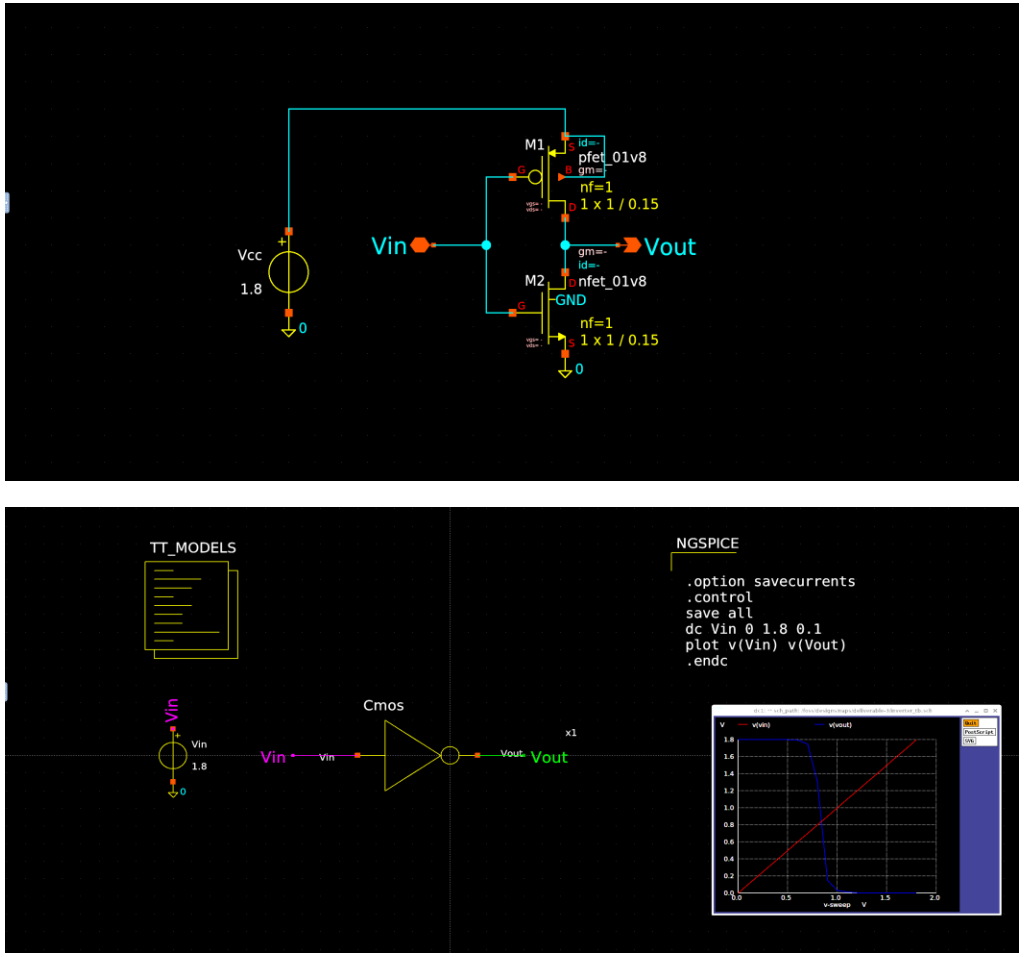
- Physical device layout to be mapped onto silicon
- Follows the Hackerfab layout
- Sky130A PDK
- PMOS and NMOS cells developed first, connected together to create CMOS
- GDS file is what actually gets sent to fab
- Design must pass DRC and LVS
  - DRC – Design Rules Constraints
    - Widths, tolerances, etc.
  - LVS – Layout Versus Schematic
    - Checks that the layout actually matches what is supposed to be designed per the device schematic



Left to right, top to bottom: PMOS, NMOS, CMOS

Schematic with xschem

- Create a CMOS schematic, symbol, and testbench with xschem
- Schematic can be used in conjunction with Klayout to pass LVS
- Modeled with PMOS and NMOS cells to achieve device design
- Testbench can then test electrical characteristics using a voltage sweep on device
- SPICE simulation



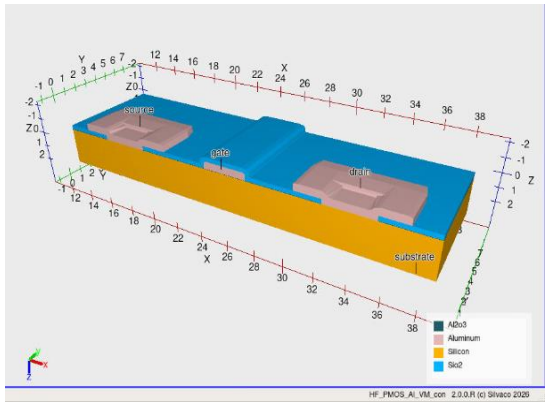
Top to bottom: schematic, testbench with electrical characteristics

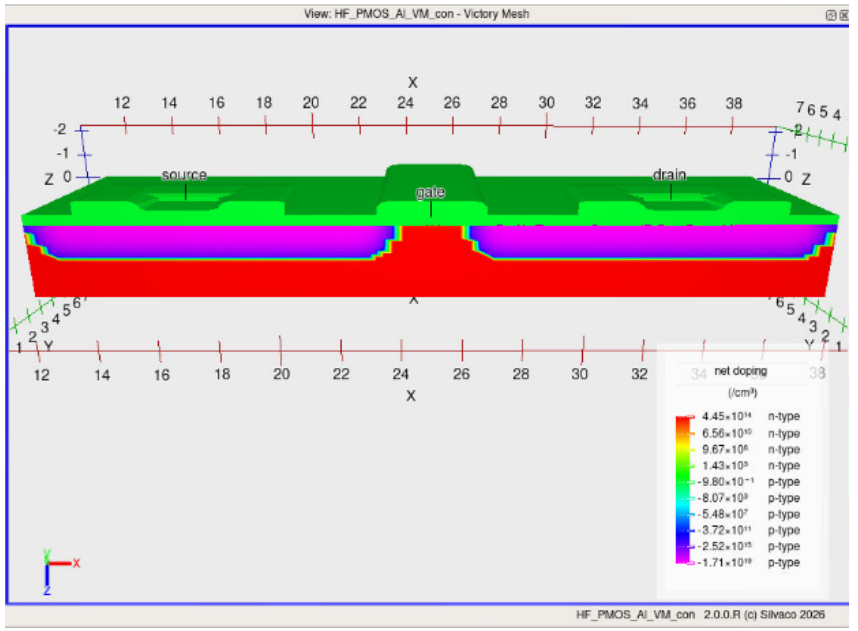
Skill 4

3D Device and Design of Experiments – Silvaco TCAD and DOE

3D Device Model in Silvaco TCAD

- 3D device process based on all Klayout GDS and prior process flow
- Heavy memory usage, device was only simulated on a slice of transistor
  - Device model was also mirrored
  - Visible jagged edges in doping view due to coarse mesh
- Process is similar to old 2D deck with updates to add variables for DOE





Top to bottom: 3D device material view, 3D device doping view

Design of Experiments in VictoryDOE

- DOE is used to rerun the deck simulation multiple different times while changing variables
- Can be used to "quickly" determine what effects device characteristics the most
- Parameters tested were concentration of the SOD, SOD time, and thickness of the Aluminum Oxide gate

	n1	n2	n3	n4	n5	n6	n7
Csod_B	5e+20	2.5e+20	7.5e+20	5e+20	5e+20	5e+20	5e+20
SDTime	30	30	30	20	40	30	30
Tal2o3	0.025	0.025	0.025	0.025	0.025	0.02	0.03

	1	2	3	4	5	6	7
1_process	7m45s	7m49s	7m51s	7m32s	7m45s	7m01s	7m00s
2_mesh	5m20s	5m15s	5m15s	5m12s	5m13s	4m24s	3m53s
3_device	17m53s	17m39s	17m53s	17m18s	17m40s	19m02s	17m58s
4_internal	5s	5s	4s	4s	5s	6s	5s
5_device	38m22s	31m29s	27m05s	27m14s	34m54s	28m40s	38m54s
6_internal	3s	3s	2s	2s	2s	2s	2s
7_device	-	-	-	-	-	-	-
8_internal	-	-	-	-	-	-	-
Total	1h09m28s	1h02m20s	58m10s	57m22s	1h05m39s	59m15s	1h07m52s

Top to bottom: process factors being tested and their values, full flow time for each cell

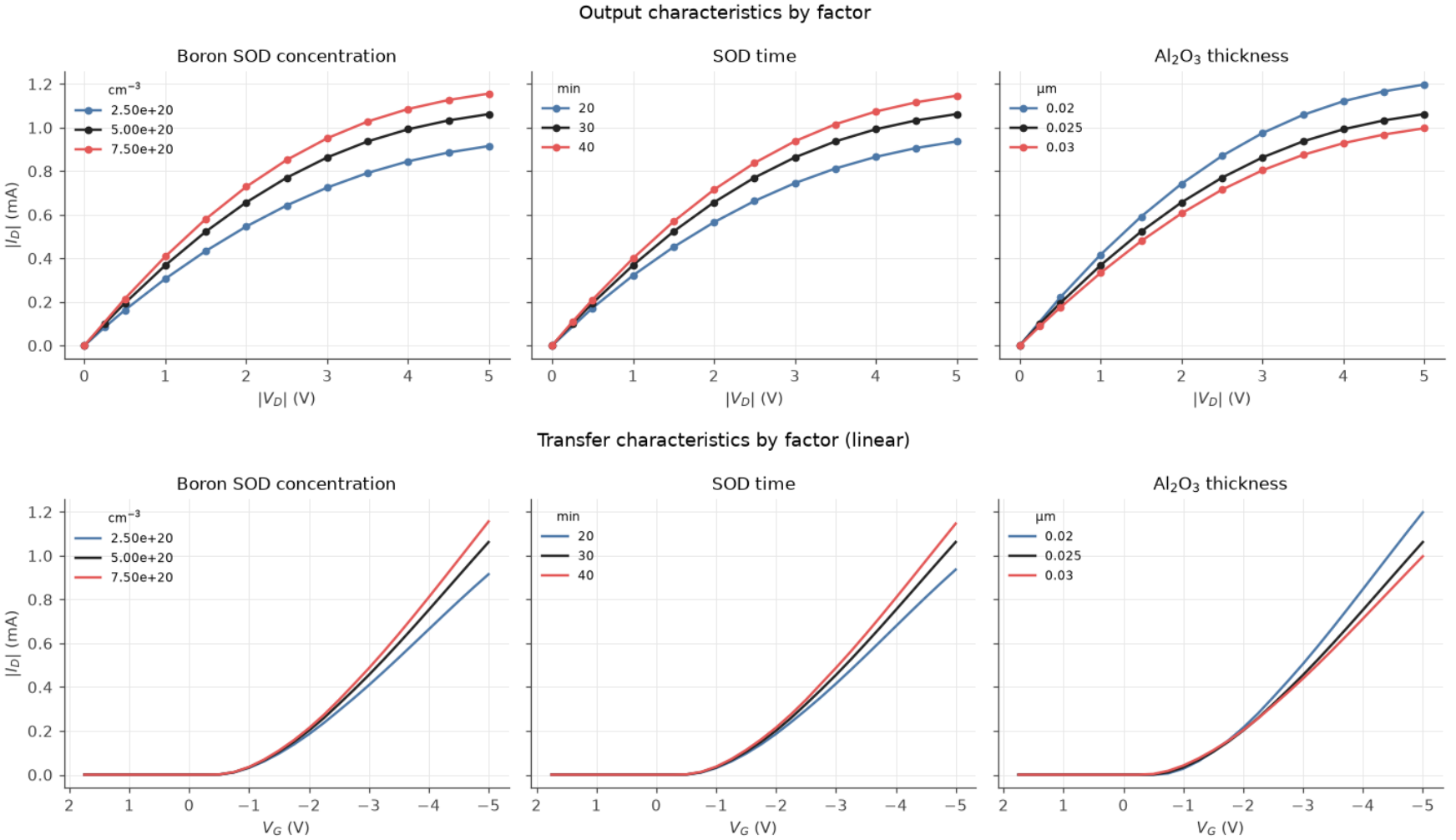
Design of Experiments in VictoryDOE

- Each process and device simulation is run to completion on the 3D device
- Output and transfer characteristics (IV curves) generated
- Many other values tested using voltage sweeps
- On and off device currents also tested

OUT:4_internal	Vtgm_V	-0.463	-0.457	-0.465	-0.463	-0.46	-0.575	-0.359
	Vtlin_V	-0.417	-0.427	-0.407	-0.441	-0.395	-0.515	-0.283
	Idlin_A	4.07e-5	3.42e-5	4.49e-5	3.65e-5	4.39e-5	4.62e-5	3.62e-5
	Idlin_uA_um	6.26	5.25	6.91	5.62	6.75	7.1	5.57
	Vtsat_V	-0.299	-0.308	-0.293	-0.317	-0.286	-0.503	-0.261
	Idsat_A	0.00106	0.000915	0.00116	0.000936	0.00115	0.0012	0.000997
	Idsat_uA_um	163	141	178	144	176	184	153
	Ioff_A	8.92e-13	7.04e-13	1.45e-12	6.27e-13	3.76e-12	6.01e-13	6.34e-12
	Ioff_pA_um	0.137	0.108	0.223	0.0965	0.579	0.0924	0.975
	SSsat_mV_dec	79	75.9	82.4	73.7	87.9	71.8	74.7
	DIBL_mV	118	119	114	124	109	11.9	21.8
OUT:6_internal	IdVd5_A	0.00106	0.000915	0.00116	0.000936	0.00115	0.0012	0.000997
	IdVd5_uA_um	163	141	178	144	176	184	153

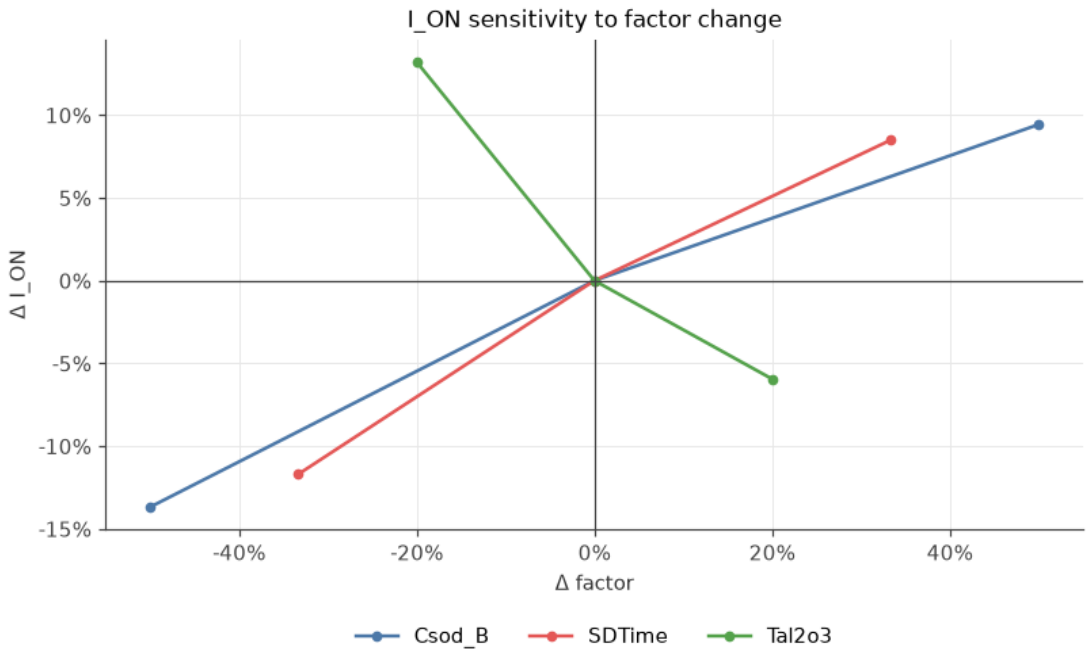
Example of an output of a DOE session

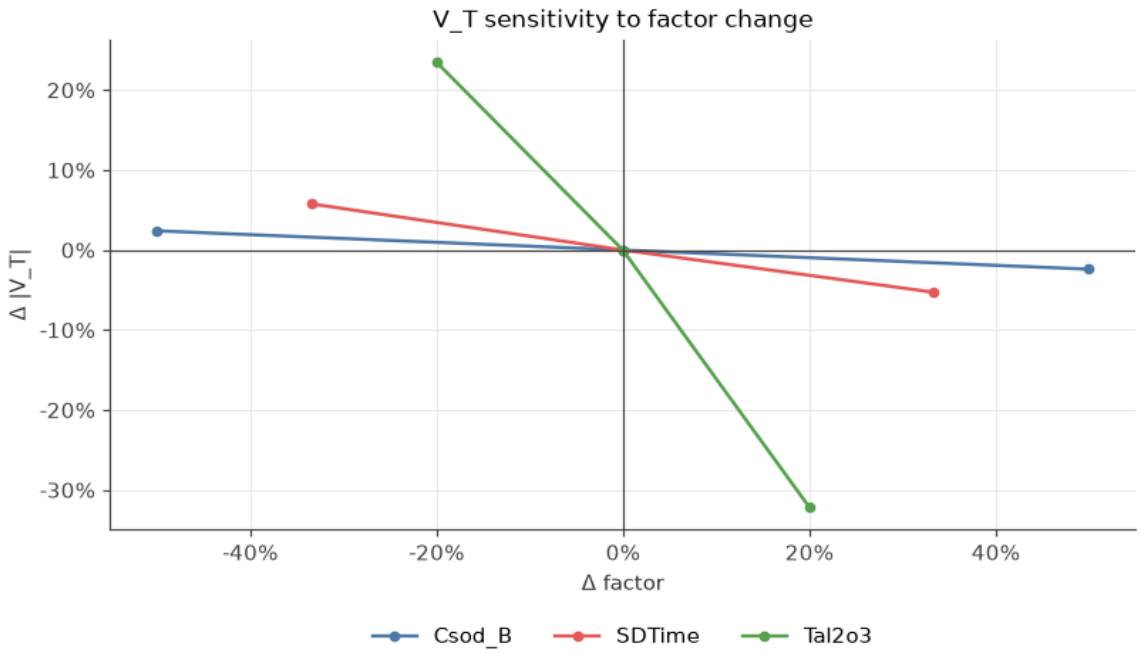
Measured Values from VictoryDOE



IV curves of device simulation showing different effects of each factor (low, baseline, high)

Sensitivity of Tested Factors





% change in select characteristics vs % change in factor